GENERATING PRB SEQUENCES FOR SYSTEM TESTING AT 500MEGABITS/SEC. AND HIGHER USING IC FLIP-FLOPS.

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ABSTRACT

Generating pseudo-random bit sequences at very high bit-rates is limited by the maximum switching speed of shift registers and modulo-2 adders. A system is proposed in which registers composed of integrated circuits, operating near their maximum bit-rate may be combined in parallel to produce sequences at much higher rates.

Introduction

In general there are two main lines of approach to the design of shift registers for use in very high speed PRBS generators. One approach is to use especially conceived circuits using high speed discrete devices in unique configurations. Examples of this method [1,2] use tunnel diode circuits in which special arrangements have to be made to overcome the set and reset problem. The former [1] requires a complex clocking waveform; the other uses pumped tunnel diode circuits and delay lines. Clearly the need for subnanosecond switching-times imposes severe restraints on the layout of such circuits.

The other line of approach is to try to use integrated circuits with their inherent layout advantages as much as possible, and only use special discrete circuits for peripheral processing. A disadvantage with ICs is having to take what is available. The work described briefly here has taken this approach, assuming that the shift registers would be composed of high-speed flip-flops with master-slave operation, typified by MECL III. This integrated circuit has a quoted maximum toggling speed of 330Mbits/sec. but in the shift register configuration a bit-rate of 160Mbits/sec. has been confirmed. The new method of generation here was developed in order to find a way of using these circuits in a configuration that would provide a substantially higher effective bit rate.

Generation Theory

The method basically involves the modulo-2 addition of an m-sequence and a delayed version of the same sequence (Fig.1.). Suppose a sequence Si is modulo-2 added to another sequence which is a replica of Si but delayed in time by J bits and a half-bit i.e. it is staggered. The output sequence must now be represented by two modulo-2 equations, namely

$$Si \oplus Si\text{-}J = Si\text{-}K \quad \ldots\ldots(1)$$

where K is a constant

and $Si \oplus Si\text{-}J\text{-}(n+1)/2^x = Si\text{-}L \quad \ldots\ldots(2)$

where L is a constant, x is an integer and $(n+1)/2^x$ is the sampling increment. It may be shown that if $L\text{-}K=(n+1)/2^{x+1}$ then the output sequence is given by,

$$Si\text{-}K,\ Si\text{-}K\text{-}\frac{n+1}{2^{x+1}},\ Si\text{-}K\text{-}\frac{2(n+1)}{2^{x+1}},\ Si\text{-}K\text{-}\frac{3(n+1)}{2^{x+1}},\ldots$$

Also J may be shown to equal $-(n+1)/2^{x+1}$...(3)

This theory may be readily applied to the case in which the outputs of two four-stage registers are modulo-2 added to give the final sequence (Fig.2). The registers may be driven by alternate clock pulses thus giving the effect of being staggered. To determine the initial loading of the second register it is first necessary to find the appropriate value of x. The original sequence i.e. that produced by the first register, has not been sampled, but is nevertheless equivalent to the sequence produced by sampling at every (n+1) bit. Since the sampling increment is defined earlier as $(n+1)/2^x$, then clearly x = 0. Therefore the initial loading of the second register must be advanced by J = (n+1)/2 = 8 (from equation 3). The output sequence is therefore given by

$$Si\text{-}K,\ Si\text{-}K\text{-}\frac{n+1}{2},\ Si\text{-}K\text{-}\frac{2(n+1)}{2},\ Si\text{-}K\text{-}\frac{3(n+1)}{2} \quad \ldots(4)$$

which is a delayed version of Si sampled at every (n+1)/2 bits; the bit-rate therefore being twice that of the generating sequencies.

A four-register configuration may also be proposed in which the sequences are modulo-2 added in pairs. The first two registers have the same initial loadings as those just discussed, but their output must now be added to the output of another pair of registers whose initial loadings must be derived.

The sampling increment of sequence (4) is (n+1)/2 which by the previous definition means that x must now be unity. It can be shown that x increases by one for each modulo-2 addition. In order to produce yet another PR m-sequence, the sequence described by (4) must be modulo-2 added to another which is advanced by

$J^1 = (n+1)2.2^x$ with x = 1, or (n+1)/4. The first term of this sequence will therefore be Si-K+(n+1)/4. This must be generated by the second pair of registers whose initial loadings we need to calculate. The equation that gives the output term Si-K+(n+1)/4 must be

$$Si + \frac{n+1}{4} \oplus Si + \frac{3(n+1)}{4} = Si\text{-}K + \frac{(n+1)}{4}$$

The registers 3 and 4 must therefore have loadings of (n+1)/4 and 3(n+1)/4. The final output sequence has a bit-rate four times that of the original sequences i.e. 640Mbits/sec. using MECL III flip-flops. The registers would be clocked in order by a four-stage ring counter.

A bit rate of 1.28Gbits/sec. is possible using eight registers driven by an eight-stage

ring counter. The loadings of the registers have been derived as:-

1st Pair:	0 and (n+1)/2 producing sequence A
2nd Pair:	(n+1)/4 and 3(n+1)/4 producing sequence B
3rd Pair:	(n+1)/8 and 5(n+1)/8 producing sequence C
4th Pair:	3(n+1)/8 and 7(n+1)/8 producing sequence D

A and B are modulo-2 added giving sequence E
C and D are added to give F
Finally E and F are added to give the output sequence with a bit-rate eight times as fast as for each individual register.

Implementation

The system described still needs very high-speed modulo-2 adders. However, the problem is alleviated by the realisation that because of the staggering of the sequences, no two sequences change at the same time. Therefore modulo-2 addition may be performed by an edge-triggered flip-flop on the transitions in the sequences rather than on the logic levels. If the transitions in the register-outputs are all very fast and clearly separated in time then just one adder will suffice, all (eight) sequences being applied directly to it.

An edge-triggered binary circuit operating at 1GHz has been described [3,4] which uses tunnel diodes and which can be triggered by positive or negative edges. The rise-times of the output pulses of each register may be improved using a tunnel diode monostable [5] with a cycle time of 300ps and a rise time of 70ps. Narrow pulses can be obtained using a strip-line differentiator [6], which is terminated in a common base transistor which in turn drives the edge-triggered binary. The general theory has been confirmed by computer search and a low-speed model of the system has been successfully implemented.

Acknowledgement.

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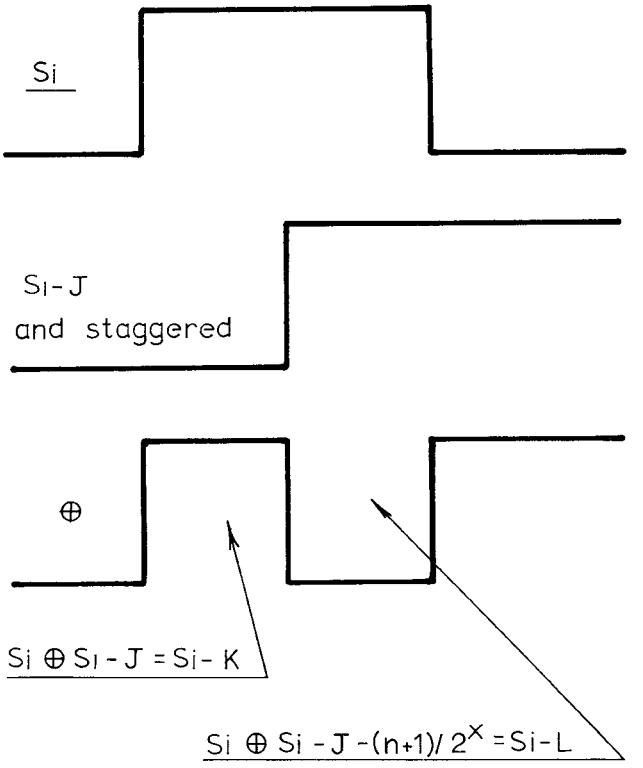

FIG.1. ADDITION OF ORIGINAL AND STAGGERED SEQUENCES.

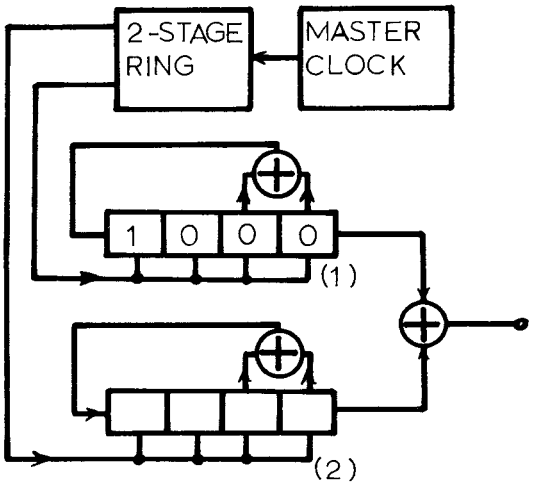

FIG.2. TWO-REGISTER GENERATOR.

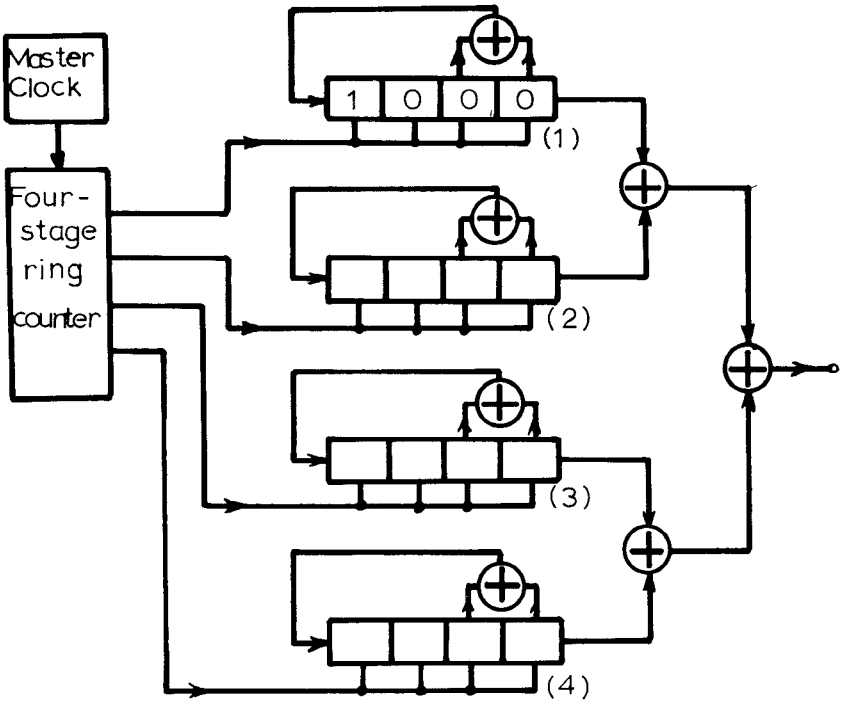

FIG.3. CONFIGURATION OF A FOUR-REGISTER GENERATOR WITH A POTENTIAL OUTPUT BIT-RATE OF 640MBITS/SEC.

NOTES